Intel® Xeon® and Intel® Xeon Phi™ Roadmap Update
Laurent Duhem
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Relative performance is calculated by assigning a baseline value of 1.0 to one benchmark result, and then dividing the actual benchmark result for the baseline platform into each of the specific benchmark results of each of the other platforms, and assigning them a relative performance number that correlates with the performance improvements reported.

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Notice revision #20110804
Transforming the Economics of HPC

Executing to Moore's Law

Predictable Silicon Track Record – well and alive at Intel. Enabling new devices with higher performance and functionality while controlling power, cost, and size.
R&D - Evaluating New Materials

Graphene

Carbon nanotubes

Molybdenum Disulfide
Driving Innovation and Integration
Enabled by Leading Edge Process Technologies

SYSTEM LEVEL BENEFITS IN COST, POWER, DENSITY, SCALABILITY & PERFORMANCE

**Future options are forecasts and subject to change without notice.

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Intel Technical Computing Portfolio

INTEL TECHNICAL COMPUTING SOLUTIONS PORTFOLIO

All components working “Better Together” for a comprehensive and high-performance end-to-end solution based on Intel technologies
Performance Technologies
Parallelism on all Levels

**NODES**
Messaging

**CORES**
Multi-Threading

**SIMD**
Vectorization

Nodes + Fabric (CLUSTER)

Multi-Core (CPU)

Many-Core (CPU)

Core

*Other names and brands may be claimed as the property of others.*
Portable & Scalable Parallel Programming
On a Higher Abstracted Level

Data-Parallelism
Vectorization
Automatic
Directives/Pragmas
Libraries

Thread/Task-Parallelism
Multi-Threading
OpenMP*
TBB, Cilk™ Plus
OpenCL
pthreads

Process-Parallelism
Message Passing
MPI
IP-based

Professional Edition
Professional Edition
Cluster Edition

128b
256b
512b
SIMD

Multicore
Many-Core
Cluster

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What is Next in HPC?

**Manycore**
- **TODAY**: Xeon Phi™ Coprocessor (22nm)
- **FUTURE**: Knights Landing Processor (14nm)
  - Knights Corner to Knights Landing sales upgrade program

**Fabric**
- **TODAY**: True Scale QDR-40/80
- **FUTURE**: Omni-Path Gen1 100Gb/s
  - True Scale Fabric to Omni-Path Fabric sales upgrade program

**Multicore**
- **TODAY**: Xeon E5 v3 Haswell-EP (22nm)
- **FUTURE**: Broadwell-EP (14nm)

All timeframes, features, products, and dates are preliminary forecasts and subject to change without further notification.

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SIMD

AVX-512
Knights Landing/
Future Xeon
512-bit

AVX2
Haswell Architecture
256-bit

AVX
Sandy Bridge Architecture
256-bit

FMA
FMA (*,+)
MUL (*) ADD (+)

All dates, product descriptions, features, availability, and plans are forecasts and subject to change without notice.
# Intel® AVX/AVX2/AVX-512

<table>
<thead>
<tr>
<th>AVX</th>
<th>AVX2</th>
<th>AVX-512</th>
</tr>
</thead>
<tbody>
<tr>
<td>256-bit basic FP</td>
<td>256-bit integer PERMD Gather Float16 (IVB 2012) 256-bit FP FMA</td>
<td>512-bit FP and Integer 32 registers 8 mask registers Embedded rounding Embedded broadcast Scalar/SSE/AVX “promotions” Native media additions HPC additions Transcendental support Gather/Scatter</td>
</tr>
<tr>
<td>16 registers</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NDS (and AVX128)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Improved blend</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MASKMOV Implicit unaligned</td>
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</tbody>
</table>
AVX** Frequency - Summary

- The Intel® Xeon® E5 v3 processor family (Haswell) now include the addition of AVX2 instructions which provides significant performance improvement as compared to non-AVX workloads.

- When executing Intel® AVX** instructions, the processor may run at less than rated frequency. To provide more information on frequencies, separate frequency specifications will be used:
  - Rated/TDP (non-AVX) frequency and turbo
  - AVX base frequency and turbo

- Performance when using AVX instructions is significantly greater than non-AVX instructions even when the processor is operating at a slightly lower frequency.

- Intel® Turbo Boost Technology continues to provide opportunistic frequency increases based on workload, number of active cores, temperature, power and current.

- Due to workload dependency, separate AVX base & turbo frequencies will be defined for Xeon® processors starting with Intel® Xeon® E5 v3 product family.

Additional Resources:
- Whitepaper - Optimize Performance with Intel AVX
- Intel® Xeon® Turbo Boost Opportunistic Frequency Upside
- Using Intel AVX to Achieve Maximum Performance on Intel Xeon Processors

**Intel® AVX refers to Intel® AVX, Intel® AVX2 or Intel® AVX-512
Tick-Tock Development Cycles
Integrate. Innovate.

Intel® Core™ Microarchitecture
- Sandy Bridge Microarchitecture
- Haswell Microarchitecture
- Future Microarchitecture

Projection

**Intel® Architecture Instruction Set Extensions Programming Reference, #319433-012A, FEBRUARY 2012**
**Intel® Architecture Instruction Set Extensions Programming Reference, #319433-015, JULY 2013**

Potential future options, subject to change without notice.
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Intel HPC Midrange Roadmap

**2015**
- **Knights Corner**
  - 22nm
  - Coprocessor
  - KNI up to 61c
  - GDDR5
  - PCIe Card

**2016**
- **Knights Landing**
  - 14nm
  - AVX-512
  - MCDRAM
  - DDR4
  - PCIe3
  - Omni-Path 1 on-pkg option

**FUTURE**
- **Future Knights**
  - 10nm
  - Knights Hill
  - Omni-Path 2

**FABRIC**
- **True Scale**
  - 40Gb
  - 80Gb Dual-Rail
  - PSM SW-Stack

- **Omni-Path Gen1**
  - 100Gb/s
  - PSM SW-Stack
  - up to 48-port switches
  - Silicon Photonics

- **Future Omni-Path**
  - Omni-Path Gen2

**XEON® E5**
- **Haswell-EP**
  - 22nm
  - up to 18c
  - AVX-2
  - DDR4
  - PCIe3

- **Broadwell-EP**
  - 14nm
  - AVX-2
  - DDR4
  - PCIe3

- **Future Xeon-EP**
  - ≤14nm

*Forecast and Estimations, in Planning & Targets*

Not drawn to scale, for illustration only. Potential future options, subject to change without notice. Codenames, for illustration only. All timeframes, features, products and dates are targets and preliminary forecasts and subject to change without further notification.
Intel Technical Computing Portfolio

- Intel® based Workstations/Visualization
- Intel® Cluster Ready (ICR)
- Intel® Data Center Manager (DCM)
- Intel® SW Development Tools
- Intel® Big Data Analytics Toolkit
- Intel® Enterprise Edition Lustre (Filesystem)
- Intel® SSD (NVM)
- Intel® based Storage
- Intel® True Scale (IBA) & Omni-Path Fabric
- Intel® Networking (GbE)
- Intel® Boards & Systems
- Intel® Xeon Phi™ Processors and Coprocessors
- Intel® Xeon® Processors

INTEL TECHNICAL COMPUTING SOLUTIONS PORTFOLIO

All components working “Better Together” for a comprehensive and high-performance end-to-end solution based on Intel technologies.
Intel® Xeon® Processors

Intel® Xeon® E3

Memory

PCIe3

Intel® Xeon® E5

Memory

PCIe3

2x QPI

Intel® Xeon® E7

Memory

PCIe3

3x QPI

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# Intel® Xeon® Processors & Platforms

<table>
<thead>
<tr>
<th>Intel® Xeon® E5-1xxx</th>
<th>Intel® Xeon® E5-2xxx</th>
<th>Intel® Xeon® E5-4xxx</th>
<th>Intel® Xeon® E7-xxxx</th>
<th>Intel® Xeon® E7-xxxx</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU/Socket</td>
<td>QPI</td>
<td></td>
<td></td>
<td>&gt;4S</td>
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</table>

- **Intel® Xeon® E5-1xxx**: CPU/Socket
- **Intel® Xeon® E5-2xxx**: QPI
- **Intel® Xeon® E5-4xxx**: QPI
- **Intel® Xeon® E7-xxxx**: >4S
- **Intel® Xeon® D**: SoC
- **Intel® Xeon® SoC**: OEM Node Controller

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The DDR4 Difference

- Next Evolution in memory technology with Higher speeds, Lower Voltage, improved density
- Sustain higher memory speed at greater memory capacities

Source as of August 2014 TR#3044 on STREAM (triad): Intel® Server Board S2600CP with two Intel® Xeon® Processor E5-2697 v2, 24x16GB DDR3-1866 @1066MHz DR-RDIMM, score: 58.9 GB/sec. New Configuration: Intel® Server System R2208WTTYS with two Intel® Xeon® Processor E5-2699 v3, 24x16GB DDR4-2133 @ 1600MHz DR-RDIMM, score: 85.2 GB/sec. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more information go to http://www.intel.com/performance. *Other names and brands may be claimed as the property of others.
Cluster on Die (COD) Mode

- Supported on 2S HSW-EP SKUs with 2 Home Agents (10+ cores)
- Targeted at NUMA workloads where latency is more important than sharing data across Caching Agents (Cbo)
  - Reduces average LLC hit and local memory latencies
  - HA mostly sees requests from reduced set of threads which can lead to higher memory bandwidth
- OS/VMM own NUMA and process affinity decisions – aka exported as 2 numa nodes
Intel® Xeon® Processor E5-2600 v3 Product Family
Memory Read Latency & Bandwidth

Source as of 17 Dec 2013: Intel internal measurements on platform with two E5-26xx v3 (14C, 2.7GHz, 145W), Turbo disabled, 8x16G DDR4-2133, RHEL 6.3. Platform with two E5-2697 v2, Turbo enabled, 8x16GB DDR3-1866, RHEL 6.3. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more information go to http://www.intel.com/performance

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## INTEL TECHNICAL COMPUTING SOLUTIONS PORTFOLIO

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Intel® Xeon Phi™ Coprocessor Product Lineup

**7 Family**
Highest Performance, Most Memory
Performance leadership

- **16GB GDDR5**
  - 352GB/s
  - >1.2TF DP
  - 270-300W
  - 7120P

**5 Family**
Optimized for High Density Environments
Performance/Watt leadership

- **8GB GDDR5**
  - >300GB/s
  - >1TF DP
  - 225-245W
  - 5110P

**3 Family**
Outstanding Parallel Computing Solution
Performance/$ leadership

- **6GB GDDR5**
  - 240GB/s
  - >1TF DP
  - 300W
  - 3120P

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Intel® Xeon Phi™ Product Family
Industry and User Momentum

1 TFLOPS
(peak F.P.-DP)
Knights Corner

3+ TFLOPS
(peak F.P.-DP)
Knights Landing

>50 Systems Provider expected\(^1\)
many more card based systems

>100 PFLOPS customer system compute commits to-data\(^1\)

H2'15 First Commercial Systems

Knights Hill

3rd Generation Intel® Xeon Phi™ Product Family
2nd Generation Intel® Omni-Path Architecture
10nm Process Technology

User Upgrade Program available TODAY

\(^1\)Intel internal estimate
Knights Landing
Next Generation Intel® Xeon Phi™

Cores based on Intel® Atom™ (Silvermont) microarchitecture with HPC enhancements:

- 14nm
- AVX-512: 512-bit SIMD (VPU)
- 4 threads/core
- deep out-of-order buffers
- gather/scatter
- better branch prediction
- higher cache bandwidth

Binary compatible with Intel® Xeon® processors:

- 60+ cores
- 3+ TFLOPS DP peak up to 3x single thread
- 2-D core mesh
- SMP cache coherency
- Intel® Omni-Path Fabric
- high performance on-package memory
- up to 16GB
- ~5x STREAM performance over DDR4
- NUMA support

Server Processor

Potential future options, subject to change without notice. Codenames.

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Intel® Omni-Path - The Next-Generation Fabric

- Designed for Maximum Scalability
- Rich Set of Programming Models
- Flexible Configurations
- End-to-End Solution

**OpenFabrics Alliance**

Starting with Knights Landing

Future Xeon

Coming in H2'2015:

- PCIe3 Adapters
- Edge Switches
- Director Systems
- Intel® Silicon Photonics
- Open Software Tools**

Intel® True Scale Fabric Upgrade Program
Helps Your Transition

**OpenFabrics Alliance**

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Goals

1. Enable developers and end customers to jumpstart code modernization efforts on Intel® Architecture through increased training availability and affordable access to Intel-based hardware and software solutions
2. Prepare for Knights Landing (KNL) by enabling software to be parallelized, vectorized and optimized on today’s Intel® Xeon Phi™ coprocessors
Intel® Code Modernization Enablement Program for Developers

Promotion on Intel® Xeon Phi™ Coprocessors 5110P and 5120D

How to redeem:
• Visit http://software.intel.com/en-us/articles/intel-code-modernization-enablement-program for a list of participating partners
• Contact your preferred OEM sales representative

Promotion on Intel® Parallel Studio XE Cluster Edition – 1 seat (80% off)

How to redeem:
• Requirement: Attend Intel® Code Modernization workshop or training webinar and purchase Intel® Xeon Phi™ Coprocessor 5110P or 5120D
• Limited to 1 license per Intel® Xeon Phi™ Coprocessor 5110P or 5120D purchased

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Meet “the book of the year”

Authors: Alexander Supalov, Andrey Semin, Michael Klemm, Chris Dahnken

Table of Contents
• Foreword by Bronis de Supinski (CTO LLNL)
• Preface
• Chapter 1: No Time to Read this Book?
• Chapter 2: Overview of Platform Architectures
• Chapter 3: Top-Down Software Optimization
• Chapter 4: Addressing System Bottlenecks
• Chapter 5: Addressing Application Bottlenecks: Distributed Memory
• Chapter 6: Addressing Application Bottlenecks: Shared Memory
• Chapter 7: Addressing Microarchitecture Bottlenecks
• Chapter 8: Application Design Implications

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